IN THE CLAIMS

Each claim of the application is set forth below with a parenthetical notation immediately following the claim number indicating the claim status. The Examiner's entry of the claim amendments under Section 1.121 is respectfully requested.

1. (ORIGINAL) An apparatus for opening an integrated circuit fuse by controllably passing current therethrough, comprising:

a controllable bulk semiconductor device;

an element for controlling an on state of the bulk semiconductor device; and

wherein current flows through the fuse in response to the on state of the bulk semiconductor device for opening the fuse.

2. (ORIGINAL) The apparatus of claim 1 wherein the bulk semiconductor device comprises a thyristor.

3. (ORIGINAL) The apparatus of claim 2 wherein the thyristor comprises four doped regions of alternating doping types forming three semiconductor junctions.

4. (ORIGINAL) The apparatus of claim 3 further comprising a bias voltage, wherein the four doped regions comprise a first and a second semiconductor junction each forward biased by the bias voltage, and a third semiconductor junction intermediate the first and the second junctions, wherein the third semiconductor junction is forward biased whenever the semiconductor device is in the on state and reverse biased whenever the semiconductor device is in an off state.

5. (ORIGINAL) The apparatus of claim 4 wherein the element for controlling the on state of the bulk semiconductor device forward biases the third semiconductor junction.

6. (ORIGINAL) The apparatus of claim 1 wherein the bulk semiconductor device comprises a first, a second and a third doped region formed in a semiconductor substrate, and wherein the semiconductor substrate comprises a fourth doped region of the bulk semiconductor device.

7. (ORIGINAL) The apparatus of claim 6 wherein the first doped region comprises a doped region of a first dopant type formed in a well of a second dopant type, and wherein the second region comprises the well of the second dopant type, and wherein the third region

comprises a substrate region of a first dopant type, and wherein the fourth region comprises a doped region of the second dopant type formed in the substrate region.

8. (ORIGINAL) The apparatus of claim 6 wherein in an off–state of the semiconductor device a junction between the first and the second doped regions is forward biased, a junction between the third and the fourth doped regions is forward biased, and a junction between the second and the third doped regions is reverse biased.

9. (ORIGINAL) The apparatus of claim 6 wherein in an on state of the semiconductor device a junction between the second and the third doped regions is forward biased.

10. (ORIGINAL) The apparatus of claim 1 wherein the bulk semiconductor device comprises doped regions formed in a CMOS semiconductor device, further comprising first, second, third and fourth doped regions, and wherein the first doped regions comprises a doped region of a first dopant type formed in a well of a second dopant type, and wherein the second region comprises the well, and wherein the third region comprises a substrate region of a first dopant type, and wherein the fourth doped region comprises a doped region of a first dopant type formed in the substrate region.

11. (ORIGINAL) The apparatus of claim 1 wherein the element for controlling the on state of the bulk semiconductor device comprises a MOSFET.

12. (ORIGINAL) The apparatus of claim 11 wherein a pn junction of the bulk semiconductor device is reverse-biased when the bulk semiconductor device is in an off state, and wherein the MOSFET is controllable to forward bias the pn junction to switch the bulk semiconductor device to the on state.

13. (ORIGINAL) The apparatus of claim 12 wherein the MOSFET comprises a gate terminal, a first source/drain terminal responsive to a trigger voltage and a second source/drain terminal connected to a doped region of the pn junction, and wherein the MOSFET turns on in response to a signal applied to the gate terminal forward biasing the pn junction in response to application of the trigger voltage to the doped region of the pn junction.

14. (ORIGINAL) The apparatus of claim 1 wherein the element for controlling the on state of the semiconductor bulk device comprises a first and a second MOSFET.

15. (ORIGINAL) The apparatus of claim 14 wherein a pn junction of the bulk semiconductor device is reverse-biased when the bulk semiconductor device is in an off state,

and wherein the first and the second MOSFETs are controllable to forward bias the pn junction to switch the bulk semiconductor device to the on state.

16. (ORIGINAL) The apparatus of claim 15 wherein the first MOSFET comprises a gate terminal, a first source/drain terminal responsive to a trigger voltage and a second source/drain terminal connected to a first doped region of the pn junction, and wherein the second MOSFET comprises a gate terminal, a first source/drain terminal connected to ground and a second source/drain terminal connected to a second doped region of the pn junction, and wherein the first and the second MOSFETs turn on in response to a signal applied to the gate terminal of the first and the second MOSFETs forward biasing the pn junction in response to application of the trigger voltage to the first doped region of the pn junction while the second doped region of the pn junction is connected to ground.

17. (ORIGINAL) An apparatus for selectively controlling current flow through an integrated circuit fuse, comprising:

a thyristor controllably responsive to the current flow;

a fuse serially connected to the thyristor; and

an element for switching the thyristor to an on state, wherein while in the on state the thyristor is responsive to the current flow such that current flows through the fuse, and wherein the fuse opens in response to the current.

18. (ORIGINAL) The apparatus of claim 17 wherein the thyristor comprises a first and a second doped region of opposite doping type forming a first semiconductor junction therebetween, and further comprises a third and a fourth doped region of opposite doping type forming a second semiconductor junction therebetween, and wherein the second and the third doped regions form a third semiconductor junction therebetween, and wherein the thyristor is in an on state when the first, the second and the third semiconductor junctions are forward biased, and wherein the thyristor is in an off state when the third semiconductor junction is reverse biased.

19. (ORIGINAL) The apparatus of claim 18 further comprising a bias voltage, wherein the first and the third semiconductor junctions are forward biased by the bias voltage.

20. (ORIGINAL) The apparatus of claim 18 wherein the element for switching the thyristor to an on state forward biases the third semiconductor junction.

21. (ORIGINAL) The apparatus of claim 18 wherein the element for switching the thyristor to the on state comprises a MOSFET.

22. (ORIGINAL) The apparatus of claim 21 wherein the MOSFET is controllable to forward bias the third semiconductor junction to switch the thyristor to the on state.

23. (ORIGINAL) The apparatus of claim 22 wherein the MOSFET comprises a gate terminal, a first source/drain terminal responsive to a trigger voltage and a second source/drain terminal connected to one of the second and the third doped regions, and wherein the MOSFET turns on in response to a signal applied to the gate terminal forward biasing the third semiconductor junction in response to application of the trigger voltage to one of the second and the third doped regions.

24. (ORIGINAL) The apparatus of claim 18 wherein the element for controlling the on state of the thyristor comprises a first and a second MOSFET.

25. (ORIGINAL) The apparatus of claim 24 wherein the first MOSFET comprises a gate terminal, a first source/drain terminal responsive to a trigger voltage and a second source/drain terminal connected to the second doped region, and wherein the second MOSFET comprises a gate terminal, a first source/drain terminal connected to ground and a second source/drain terminal connected to the third doped region, and wherein the first and the second MOSFETs turn on in response to a signal applied to the gate terminal of the first and the second MOSFETs forward biasing the third semiconductor junction in response to application of the trigger voltage to the second doped region while the third doped region is connected to ground.

26. (ORIGINAL) The apparatus of claim 17 wherein the thyristor comprises a first, a second and a third doped region formed in a semiconductor substrate, and wherein the semiconductor substrate comprises a fourth doped region of the thyristor.

27 (ORIGINAL) The apparatus of claim 26 wherein the first doped region comprises a doped region of a first dopant type formed in a well of a second dopant type, and wherein the second region comprises the well of the second dopant type, and wherein the third region comprises a substrate region of a first dopant type, and wherein the fourth doped region comprises a doped region of the second dopant type formed in the substrate region.

28. (ORIGINAL) The apparatus of claim 27 wherein the first, the second, the third and the fourth doped regions are formed in a CMOS semiconductor device.

29. (ORIGINAL) A memory array comprising

a plurality of addressable rows;

a plurality of addressable columns;

a memory cell at an intersection of each row and column;

wherein each memory cell further comprises;

an integrated circuit fuse;

an apparatus for opening the integrated circuit fuse, further comprising:

a current source;

a controllable bulk semiconductor device; and

wherein current flows into the fuse in response to an on state of the bulk semiconductor device for opening the fuse.

30. (ORIGINAL) A method for opening an integrated circuit fuse by controllably passing current through a bulk semiconductor device connected in series with the fuse, wherein the bulk semiconductor device comprises a plurality of semiconductor pn junctions, the method comprising:

forward biasing the plurality of semiconductor pn junctions to allow current flow through the bulk semiconductor device to the fuse for opening the fuse; and

reverse biasing at least one of the plurality of semiconductor pn junctions to prevent current flow through the bulk semiconductor device for retaining the fuse in a closed state.

31. (ORIGINAL) The method of claim 30 wherein the step of forward biasing further comprises:

switching a MOSFET to an on state, wherein the MOSFET is connected to a doped region of the reverse biased semiconductor pn junction; and

applying a forward bias voltage to the doped region through the MOSFET.

32. (ORIGINAL) The method of claim 30 wherein the bulk semiconductor device comprises a thyristor.

33. (WITHDRAWN) A method for forming a fuse and a bulk semiconductor device for opening the fuse in a semiconductor substrate, comprising:

doping the semiconductor substrate a first dopant type;

forming a well of a second dopant type in the substrate;

forming a first doped region of the first dopant type in the well;

forming a second doped region of the second dopant in the substrate;

wherein the substrate, the well, the first doped region and the second doped region form the bulk semiconductor device;

forming one or more conductive interconnect layers overlying the substrate;

forming the fuse in one of the one or more conductive interconnect layers;

electrically connecting the fuse in series with the bulk semiconductor device.

34. (WITHDRAWN) The method of claim 33 further comprising;

forward biasing semiconductor junctions formed by the substrate, the well, the first doped region and the second doped region;

passing current through the forward biased semiconductor junctions to the fuse for opening the fuse.

35. (WITHDRAWN) The method of claim 34 further comprising reverse biasing at least one of the semiconductor junctions formed by the substrate, the well, the first doped region and the second doped region to prevent current from flowing through the bulk semiconductor device to the fuse, such that the fuse remains in a closed state.